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Mullard Solid Aluminium Electrolytic Capacitors

M. G. SAGE
Industrial Markets Division, Mullard Ltd.

Recent developments in the construction of Mullard solid aluminium electrolytic capacitors have enabled larger capacitance values to be produced, with considerable price advantage over solid tantalum types. The construction, performance, service-life and reliability of these capacitors are considered.

INTRODUCTION

Solid aluminium capacitors have always offered certain advantages over other electrolytic capacitors and have been available from Mullard Ltd. since 1962. Recent developments, however, have made possible the production of these capacitors in larger can-sizes than has hitherto been technically feasible. There is therefore now a further notable advantage, namely, that the price differential between solid aluminium and solid tantalum electrolytic capacitors (in favour of solid aluminium) has been greatly increased. For example, a large can-size solid aluminium capacitor may cost only one-third of the price of a comparable solid tantalum type.

This article describes the method of producing solid aluminium capacitors, and gives information concerning the performance of these components compared with wet aluminium and solid tantalum types. Life and reliability figures are also given. Selected information about solid aluminium capacitors has already been given in Ref. 1.

CONSTRUCTION

The internal construction of the solid aluminium capacitor is shown in Fig. 1, and the manufacturing steps can be followed from Fig. 2. The curves shown in Fig. 3 indicate the relative prices of electrolytic capacitors.

The two electrodes of the solid aluminium capacitor consist of etched aluminium foil. One of these foils, the anode, is attached to an aluminium rod which is used as a central former in the winding process and also as the anode connection to the capacitor. The second foil, the cathode, has a strip tag attached to one end to serve as the cathode connection. To separate the electrodes, two strips of woven glass-wool are utilised: these will be used later to carry the necessary chemical (manganese nitrate, $Mn(NO_3)_2 . 4H_2O$) from which the non-liquid connection to the dielectric is formed during construction.

After the winding is completed, the next stage in the manufacturing process is the forming of the dielectric (aluminium oxide) on the anode foil. The core is then impregnated with manganese nitrate which is retained by the woven glass wool. A process of controlled pyrolysis is then applied to the core so that the manganese nitrate is decomposed into manganese dioxide, and into gases which must escape from the core. This pyrolysis must be performed in a particular way or the escaping gases, which include water, and both nitric and nitrous fumes, attack the aluminium oxide layer and the underlying aluminium. Since most of the damage to the foil occurs while both water and the nitric and nitrous fumes are present, and since water vapour alone comes off at temperatures below 80°C, the temperature of the core is held at 80°C long enough for almost all the water to escape, before being raised to higher temperatures to drive off the other fumes. The oxide layer sustains very little erosion by this method, and, after the pyrolysis is completed, can be repaired and re-formed in the usual way.

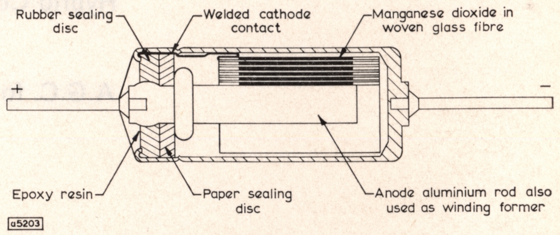
Rubber sealing disc
Welded cathode contact
Manganese dioxide in woven glass fibre
+
−
Epoxy resin
Paper sealing disc
Anode aluminium rod also used as winding former
a5203

Fig. 1—Cross-section of a solid aluminium capacitor

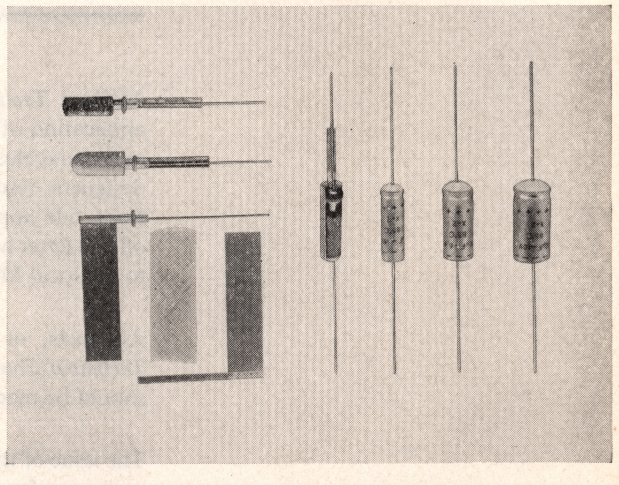

Fig. 2—Stages in the production of solid aluminium capacitors (approximately half-size)

At this stage, all that is required is encapsulation. A rubber coated s.r.b.p. disc is used at one end (anode) and the final hermetic sealing is made with epoxy resin.

The recent developments which have enabled the construction of larger can-sizes than were previously possible, consist of the production and utilisation of suitably etched aluminium foil of considerably smaller thickness. Methods have also been discovered to avoid cracking the oxide layer during manufacture, a problem that only became serious as larger can-sizes and larger 'rolls' of foil were required. The solution of these problems has made possible the large can-sizes now available, at a comparatively low price.

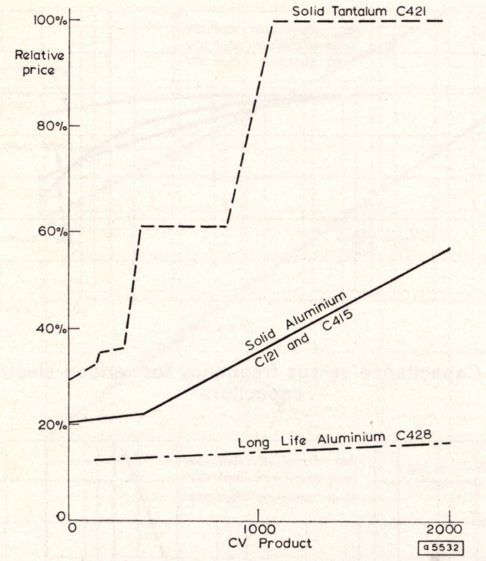

Fig. 3—Relative prices of various electrolytic capacitors

Solid aluminium capacitors are now available from Mullard Ltd. with CV product values up to 2200. In general the solid aluminium capacitor compares favourably in performance with solid tantalum slug capacitors, but is less expensive. The following paragraphs give performance details for comparison of solid aluminium, solid tantalum and long-life wet aluminium electrolytic capacitors.

PERFORMANCE

A general treatment of the theory and equivalent circuit of electrolytic capacitors has been given in Ref. 1, and serves to explain the variations of parameters which are described below.

Impedance

The effect of temperature on the impedance of solid aluminium capacitors is shown in Fig. 4a, and, for comparison, the effect of temperature on the impedance of wet aluminium capacitors is shown in Fig. 4b, and of solid tantalum in Fig. 4c. From these graphs it can be seen that, for example, a 25μF capacitor of any type would have an impedance of about 7 to 8Ω at 25°C and at 1kHz. At the higher frequency of 100kHz, but still at 25°C, the impedance of the wet type is about 2·5Ω, and that of the solid types is about 0·3Ω. There is thus, so far, little difference between the capacitors. However, if the 100kHz impedance is measured at −40°C, the impedance of the wet type will have risen by a factor of over 100, while that of the solid types will have risen by a factor of only 2.

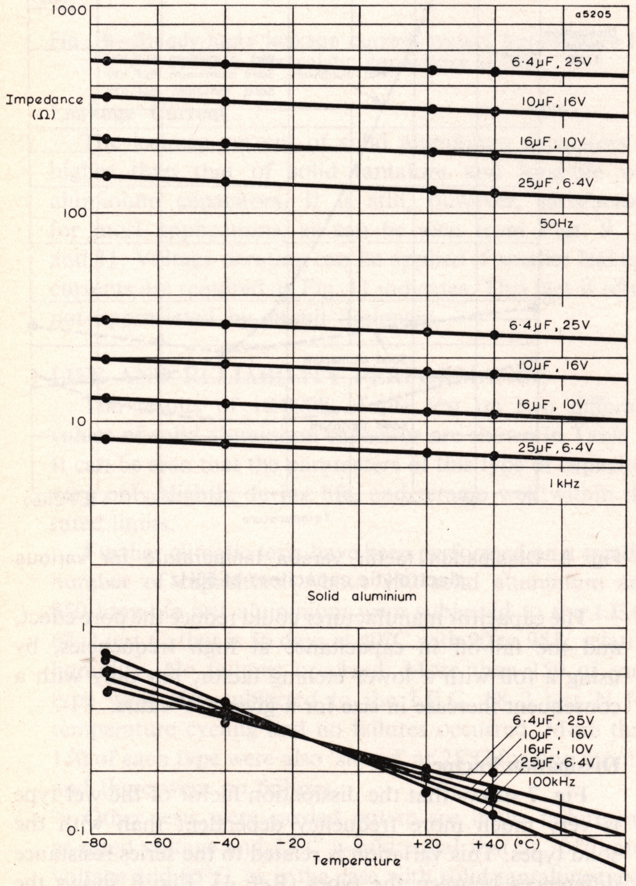

Fig. 4a—Impedance versus temperature for solid aluminium capacitors at various frequencies

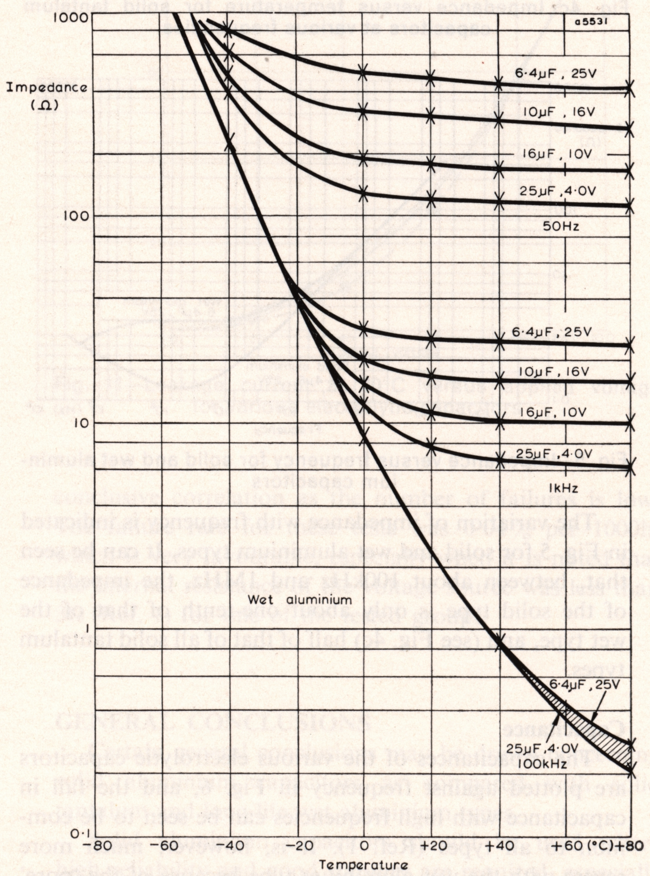

Fig. 4b—Impedance versus temperature for wet aluminium capacitors at various frequencies

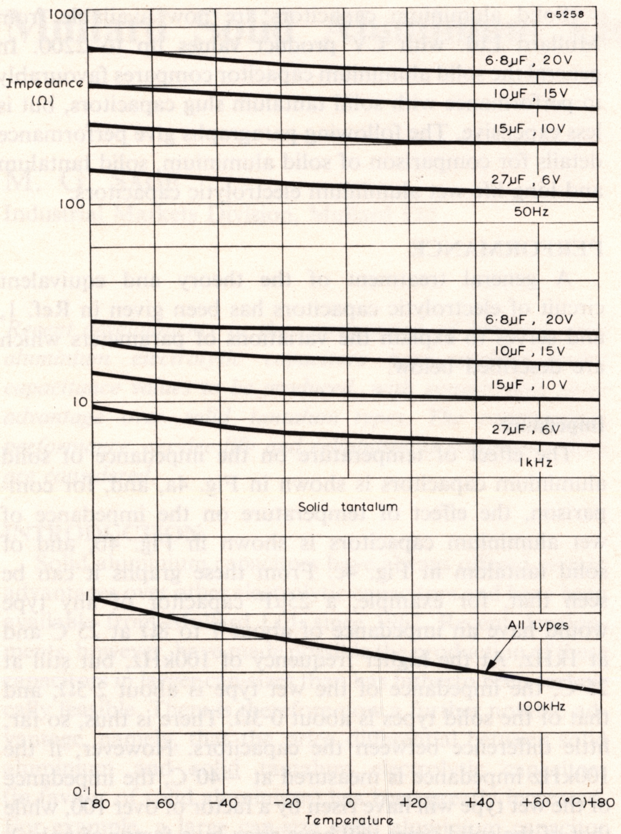

Fig. 4c Impedance versus temperature for solid tantalum capacitors at various frequencies

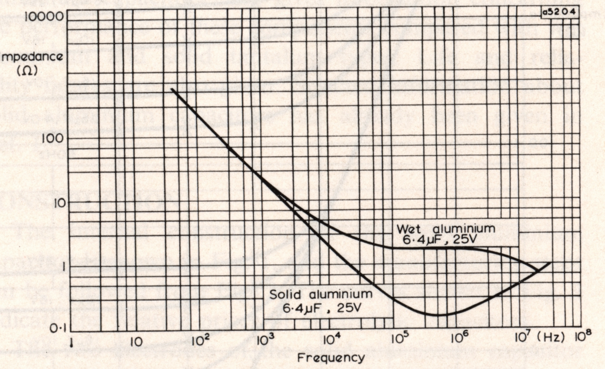

Fig. 5—Impedance versus frequency for solid and wet aluminium capacitors

The variation of impedance with frequency is indicated in Fig. 5 for solid and wet aluminium types. It can be seen that, between about 100kHz and 1MHz, the impedance of the solid type is only about one-tenth of that of the wet type, and (see Fig. 4c) half of that of all solid tantalum types.

Capacitance

The capacitances of the various electrolytic capacitors are plotted against frequency in Fig. 6, and the fall in capacitance with high frequencies can be seen to be common to all types (Ref. 1). It is, however, much more severe with the wet aluminium type because of the 'pore' effect, described under 'Operation' on page 276 of Ref. 1.

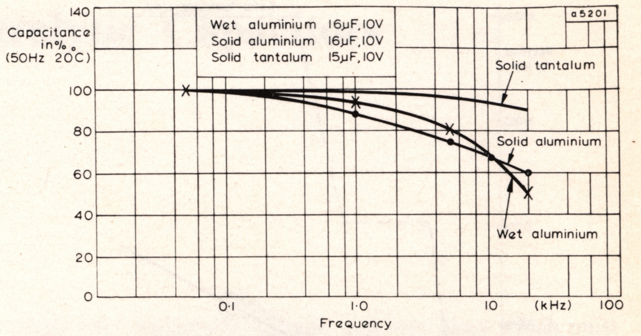

Fig. 6—Capacitance versus frequency for various electrolytic capacitors

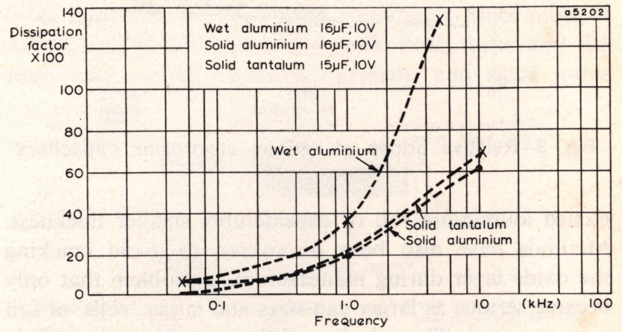

Fig. 7—Dissipation factor versus frequency for various electrolytic capacitors at 20°C

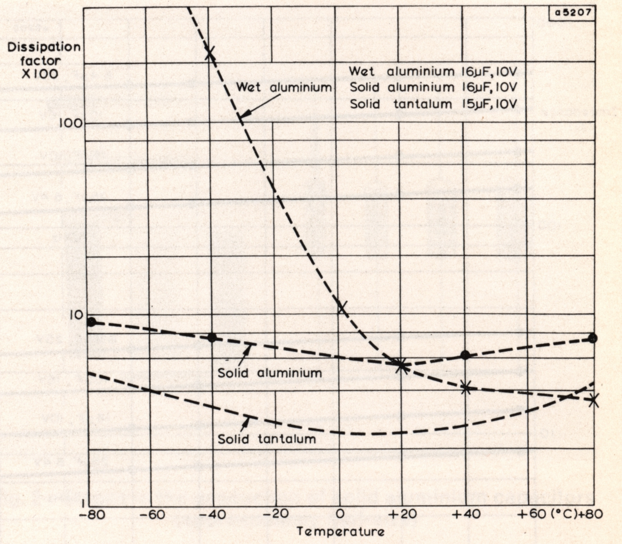

Fig. 8—Dissipation factor versus temperature for various electrolytic capacitors at 50Hz

The capacitor manufacturer could reduce the pore effect, and the fall-off in capacitance at high frequencies, by using a foil with a lower etching factor, but only with a consequent increase in size for a given CV value.

Dissipation Factor

Fig. 7 shows that the dissipation factor of the wet type is very much more frequency dependent than with the solid types. This variation is related to the series resistance differences between the types (Ref. 1). Fig. 8 shows the dissipation factor variations with temperature.

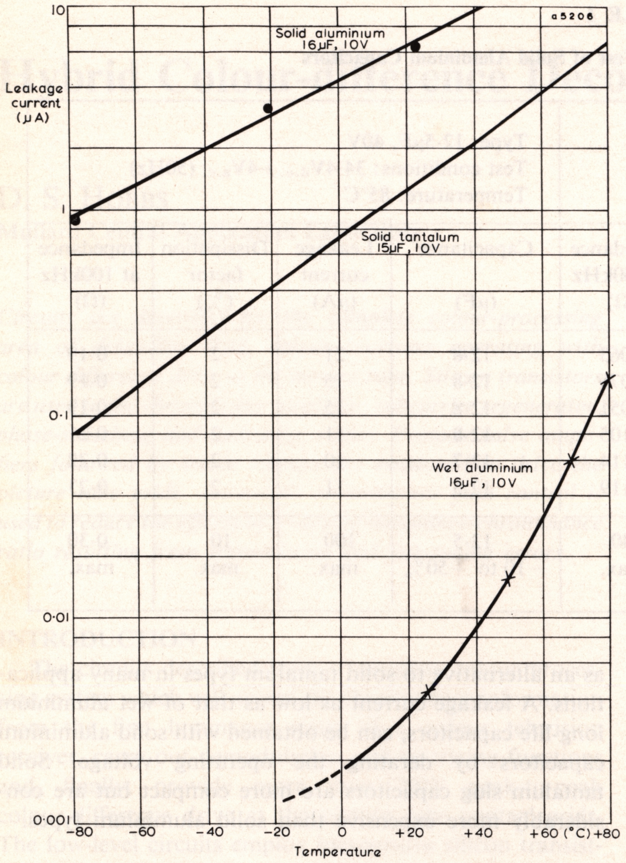

Fig. 9—Steady-state leakage current versus temperature for various electrolytic capacitors at 10V

Leakage Current

The leakage current of solid aluminium capacitors is higher than that of solid tantalum and long-life wet aluminium capacitors. It is still, however, satisfactory for most applications, as can be seen from Figs. 9, 10 and 11. Voltage derating can be applied if smaller leakage currents are required as Fig. 11 indicates. This fact is often not appreciated by circuit designers.

LIFE AND RELIABILITY PERFORMANCE

The results of 10 000h of life test on two different values of solid aluminium capacitor are shown in Table 1. It can be seen that the parameters of this type of capacitor vary only slightly during life, and remain well within the rated limits.

Further climatic tests have been performed on a smaller number of capacitors. About 350 solid aluminium and 350 long-life wet aluminium were subjected to the I.E.C. 68–2 test C, that is 56 days at 40°C with 90 to 95% relative humidity. No failures occurred. More than 150 of each type were also subjected to the I.E.C. 68–2 test N for temperature cycling and no failures occurred. More than 150 of each type were also 'stored' at 25°C for one month, and there were no failures.

Other tests were carried out to see if the failure rate at rated voltage and 25°C would equal that at 70% rated voltage and 85°C, as is the case with solid tantalum types. The results summarised in Table 2 have not yielded a conclusive correlation as the number of failures is low. The failure rate for these tests was 0·04% per 1000h, which is very favourable, especially when it is noted that the internal resistance of the voltage source was less than 3Ω (Ref. 1) for one of the tested groups.

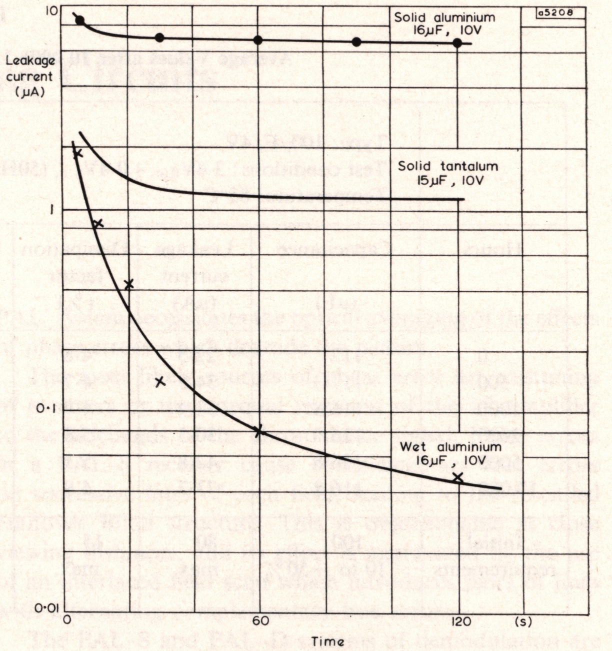

Fig. 10—Leakage current at 20°C versus time at full working voltage for various electrolytic capacitors

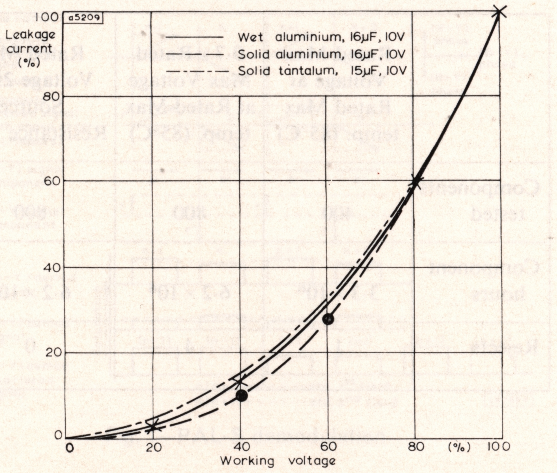

Fig. 11—Leakage current at 20°C versus applied voltage for various electrolytic capacitors

GENERAL CONCLUSIONS

Certain general conclusions may be drawn concerning solid aluminium capacitors as compared with solid tantalum and long-life wet aluminium types.

Solid aluminium capacitors should be used where high reliability and good stability are required, especially if severe environmental conditions are likely. They serve

TABLE 1

Average Values after 10 000h Life Test of Solid Aluminium Capacitors

	Type: 100μF, 4V Test conditions: $3{\cdot}4V_{d.c.}+0{\cdot}4V_{a.c.}$ (50Hz) Temperature: 85°C				Type: 12·5μF, 40V Test conditions: $34{\cdot}4V_{d.c.}+4V_{a.c.}$ (50Hz) Temperature: 85°C			
Hours	Capacitance (μF)	Leakage current (μA)	Dissipation factor (%)	Impedance at 100kHz (Ω)	Capacitance (μF)	Leakage current (μA)	Dissipation factor (%)	Impedance at 100kHz (Ω)
0	117	22·5	4·8	0·063	12·8	21	2	0·19
500	117·3	34·5	4·7	0·075	12·8	15	2	0·19
1000	116·8	33·4	4·9	0·051	12·8	15	2	0·19
2000	116·9	30·3	5·8	0·105	12·8	11	2	0·21
5000	116·8	42·8	5·3	0·114	12·7	10	2	0·22
10 000	116·8	73·7	4·8	0·119	12·5	11	2	0·23
Initial requirements	100 −10 to +50%	80 max.	15 max.	0·30 max.	12·5 −10 to +50%	100 max.	10 max.	0·30 max.

TABLE 2

Life Tests on Solid Aluminium Capacitors

	Rated Max Voltage at Rated Max temp. (85°C)	0·7×Rated Max Voltage at Rated Max temp. (85°C)	Rated Max Voltage 25°C Source Resistance <3Ω
Components tested	400	800	800
Component hours	$3{\cdot}3\times10^6$	$6{\cdot}2\times10^6$	$6{\cdot}2\times10^6$
Rejects	1	4	0

as an alternative to solid tantalum types in many applications. A leakage current as low as that of wet aluminium long-life capacitors, can be obtained with solid aluminium capacitors by derating the operating voltage. Solid tantalum slug capacitors are more compact but are considerably more expensive than solid aluminium types.

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1. Sage, M. G., 'Service-life and Reliability of Mullard Electrolytic Capacitors', **Mullard Technical Communications,** Vol. 8, No. 79, January 1966, pp. 275 to 282.
2. Boone, S., Voeten, H., Hendriks, H., 'An Aluminium Solid Electrolytic Capacitor', **IEEE Transactions of the Professional Technical Group on Component Parts,** Vol. CP-10, No. 1, March 1963.

ACKNOWLEDGEMENT

The curves shown in Figs. 4a, 4b, 4c, 6, 7, 8, 9, 10 and 11 were first published in Ref. 2.

Hybrid Colour-difference Decoding Circuits

D. S. Hobbs

Mullard Central Application Laboratory

Circuits are described for the complete colour-processing area of delay-line PAL colour receivers operating with colour difference drive to the picture tube. Silicon transistors are used in the chrominance amplifier, subcarrier regenerator, phase-switching and matrixing stages. Pentode valve amplifiers followed by triode clamps are employed to drive the picture tube grids. Automatic chrominance gain control is used to reduce the effects of a varying luminance-chrominance ratio resulting from transmission and fine-tuning errors.

INTRODUCTION

The circuits described form a complete colour processing system which will accept the chrominance information from the first luminance stage of a colour television receiver, carry out demodulation and matrixing functions and, finally, provide more than 200V peak-to-peak colour-difference drive at the picture tube control grids. The low-level circuits employ inexpensive silicon transistors and, where possible, aperiodic transformer couplings (see page 118). It is also advantageous to use transistors in these circuits from the point of view of stability, ease of adjustment and freedom from interaction. But in the output stages it is at present more economical to employ valves.

The introduction of the PAL system of colour transmission has made it necessary to include circuits for subcarrier reference phase switching and switch phase identity in the colour circuits together with the usual subcarrier regenerator, demodulator, matrix and colour-difference output stages. The chrominance amplifier has been designed to work into an ultrasonic glass delay line to provide PAL–D decoding and demodulation. The delay line is ground in the factory to the exact delay (63·943μs) and is included in a new circuit which requires no additional padding delay.

Phase switching on alternate lines is achieved by the use of a diode switch controlled by a bistable circuit. The system is driven from the line timebase; the phase of switching is checked by reference to the swinging colour burst.

Matrixing for the green colour-difference signal is carried out in a three-transistor driver amplifier which is interposed between the demodulators and the valve output stages. Triode clamps are used at the grids of the picture tube to ensure good grey-scale tracking.

PAL SYSTEM

PAL system transmissions may be received and decoded by either of two methods: 'Simple PAL' (PAL-S) and 'Delay-line PAL' (PAL-D) (Refs. 1 and 2), both of which provide cancellation of phase errors which may occur during transmission and reception. However, the 'Simple PAL' system necessitates the optical averaging of the effects of phase errors which degrade the picture.

The most likely sources of phase error are mistuning of receivers or the unequal response of the i.f. amplifier to the sidebands of the chrominance signal. Phase errors in a PAL–S receiver cause complementary hue errors on successive lines of each field, leading to the so-called Hanover Blind structure. This is objectionable at close viewing distances, and its effect is aggravated by the use of an interlaced field scan which introduces pairs of lines with alternating complementary hue errors.

The PAL–S and PAL–D systems of demodulation are explained graphically in Figs. 1 and 2, where the mean chrominance phase during each line of scan is represented by a phasor.

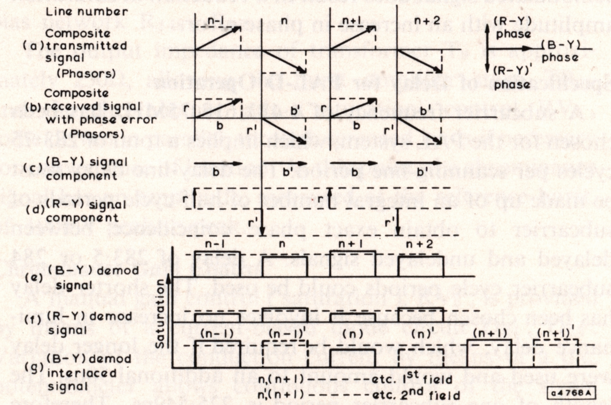

Fig. 1—PAL-S demodulation

In Fig. 1a it is shown that the phase of the R–Y component is alternated on successive lines. The same signal with constant phase error on successive lines is shown in Fig. 1b and is separated into B–Y and R–Y components in Figs. 1c and 1d. The results of synchronous demodulation are shown in Figs. 1e and 1f which demonstrate the amplitude variation which produces the Hanover Blind effect. Finally, the effect of interlace is shown in Fig. 1g. The paired amplitude error formation can be clearly seen.

The PAL–D system does not introduce the Hanover Blind effect since phase-error cancellation is carried out electronically in the delay-line circuit so that the chrominance signal is phase corrected before demodulation. The principles of PAL–D operation are shown in the sequence Figs. 2a to 2e in which the chrominance signals as received and delayed by one line period are added and subtracted vectorially at standard amplitudes. In Fig. 2a is shown the undelayed signal phasor diagrams for four lines of scan, and in Fig. 2b are shown the corresponding phasors for

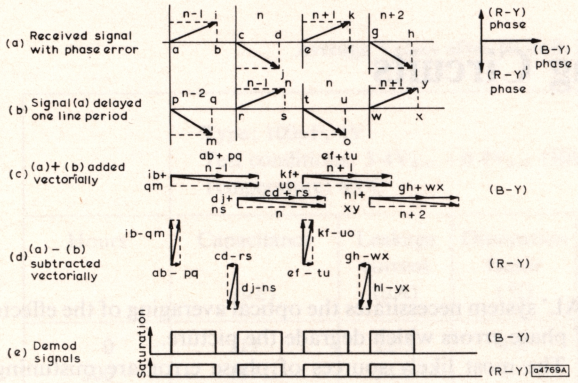
(a) Received signal with phase error
(b) Signal (a) delayed one line period
(c) (a) + (b) added vectorially
(d) (a) − (b) subtracted vectorially
(e) Demod signals
n-1
n
n+1
n+2
n-2
a
b
c
d
e
f
g
h
i
j
k
l
m
n
o
p
q
r
s
t
u
w
x
y
ab + pq
ef + tu
ib+ qm
kf+ uo
dj+ ns
cd + rs
hl+ xy
gh + wx
ib-qm
kf-uo
ab - pq
cd-rs
ef - tu
gh-wx
dj-ns
hl-yx
Saturation
(R-Y) phase
(B-Y) phase
(R-Y) phase
(B-Y)
(R-Y)
(B-Y)
(R-Y)
(B - Y)
(R - Y)
a4769A

Fig. 2—PAL-D demodulation

the delayed signals. In Fig. 2c are shown the resultant phasors obtained by vector addition of delayed and undelayed signals which produce predominantly B–Y phase signals. Similarly in Fig. 2d are shown the results of subtraction which are predominantly in the R–Y phase. Fig. 2e shows the resultant colour difference signals, of constant amplitude, from line to line.

It should be noted that there is no difference in the combined signal amplitudes from line to line. Thus no Hanover Blind effect can occur, but phase error in the demodulated signal does result in a reduction in saturation amplitude with an increase in phase error.

Specification of Delay for PAL-D Operation

A subcarrier frequency of 4·433 618 75MHz has been chosen for the PAL system, which implies a total of 283·75 cycles per scanning-line period. The delay-line delay must be made up of an integral number of half-cycle periods of subcarrier to obtain exact phase coincidence between delayed and undelayed signals. A delay of 283·5 or 284 subcarrier cycle periods could be used. The shorter delay has been chosen because it involves no increase in luminance delay, which would be required if the longer delay were used and would amount to an additional 50ns. The length of one subcarrier period is 225·549ns. Therefore the delay must be 63 943·0ns. Indications are that, to maintain satisfactory performance, the delay line must have a tolerance of ±5ns to allow for changes due to all causes within the temperature range of the receiver.

DECODER

The system is best explained initially by reference to the block diagram shown in Fig. 3 which indicates the general layout of the circuit diagram of Fig. 4. There are two main paths through the system, the reference path and the chrominance path. These diverge from the two common stages at the bottom left-hand part of Fig. 3.

Initially, the chrominance signal is extracted from the composite detected luminance signal by the chroma take-off network which feeds the controlled chrominance amplifier. Automatic chrominance control (a.c.c.) is applied to this stage to maintain a constant reference colour-burst amplitude and to provide a constant source of chrominance signal.

From the reference path at the top of the diagram, it is seen that the complete chrominance signal is amplified in the first colour-burst amplifier which feeds the burst gate amplifier which, in turn, drives the reference phase detector. A sample of the burst signal is taken to the a.c.c. detector for control purposes.

The phase detector produces a d.c. signal by phase-sensitive detection of the swinging colour burst. The d.c. control signal is smoothed by the low-pass filter which is included to control the pull-in characteristics and reduce the effects of noise. After d.c. amplification, the d.c. signal is used to control the variable-capacitance diode which, in turn, controls the phase of the crystal oscillator.

The residual 7·8kHz ripple from the detector is employed to drive a phase-checking circuit consisting of a tuned 7·8kHz amplifier and emitter follower which also drives a colour-killer bias circuit. An economy in components has been achieved by combining the function of phase checking with that of colour killing when monochrome transmissions are received.

The reference signal from the crystal oscillator is distributed by an emitter-follower buffer stage to the phase detector, the subcarrier phase switch (PAL switch), and the 90° phase shifter.

The chrominance signal path at the bottom of the diagram consists of a chroma gain control (saturation) which determines the proportion of the a.c.c. controlled signal fed to the chroma amplifier proper. A delay-line driver amplifier provides both a high-impedance current source for the delay line, which is terminated at the sending end by a 150Ω resistor, and an undelayed signal for the comparator network.

Following the delay-line circuit, the R–Y and B–Y components of the chrominance signal are separated and fed to two diode-bridge synchronous demodulators. After passing through low-pass filters which remove the subcarrier frequency, the colour-difference signals are amplified to a sufficient level to drive the valve output stages. An emitter-matrixed G–Y matrix amplifier provides the green colour-difference signal which is further amplified by a similar valve output stage.

Three driven clamps are used at the grids of the colour picture tube. These are provided conveniently by using the triode sections of the triode-pentode valves used as colour-difference amplifiers.

CHROMINANCE AMPLIFIER

Bandwidth

The R–Y and B–Y components of the transmitted signal are, at present, limited in bandwidth to the 'I' signal bandwidth as used for N.T.S.C. transmissions. If a band-pass (double sideband) of ±1MHz overall at −6dB is achieved, then a very satisfactory colour picture will be obtained. This implies that the delay line and chrominance amplifiers must each have a 3dB bandwidth of at least ±1MHz centred on 4·43MHz. The Mullard glass delay line has this specification when terminated at both ends by 150Ω resistors.

To achieve an overall bandwidth of ±1MHz at the demodulators, the chrominance amplifier is designed for a 3dB bandwidth of approximately ±1·2MHz.

Chrominance Take-off Circuit

The chrominance signal is separated from the luminance signal by a high-pass filter consisting of C_{37}, R_{36} (Fig. 4). A composite luminance signal of 3V black-to-white amplitude will provide adequate chrominance drive (chrominance amplitude 0·25V peak-to-peak burst signal). This circuit can be driven conveniently from the emitter of the luminance phase splitter used for dual-standard purposes. The rising response of the R–C filter with frequency is chosen to compensate for the falling i.f. response in the subcarrier region.

Automatic Chrominance Control (A.C.C.)

The chrominance signal amplitude will vary with receiver fine-tuning, propagation conditions, and contrast-control setting. The effects of these variations make it difficult to obtain steady subcarrier reference synchronisation and a proper proportion of chrominance-to-luminance drive at the picture tube electrodes. With a.c.c., however, the signal-level variation at the output of transformer T_9 is held within 1·5dB for 12dB variation in chrominance signal amplitude.

The first amplifier stage TR_{18} is gain-controlled for a.c.c. purposes and is common to both the reference-burst amplifier and the chrominance amplifier proper. To prevent overloading, the signal voltage at the base of TR_{18} must not exceed 100mV peak-to-peak.

A d.c. automatic-chrominance-control voltage derived from the reference-burst amplifier is applied to the base bias network R_{148}, R_{82}.

The output impedance of transformer T_9 is approximately 250Ω, allowing the burst amplifier stage TR_{19} and the chrominance gain ('saturation') control, RV_2, to be driven in parallel, through screened leads if necessary for convenience of location. At this point, the chrominance signal has an amplitude, measured at the reference burst, of 100mV peak-to-peak.

Chrominance Gain Control

A manual gain control ('saturation'), RV_2, is provided by means of a current-biased diode circuit D_{24}, D_{25}. Variation of the conduction current by means of a d.c. potentiometer allows continuous control of the signal amplitude fed to the chrominance amplifier proper

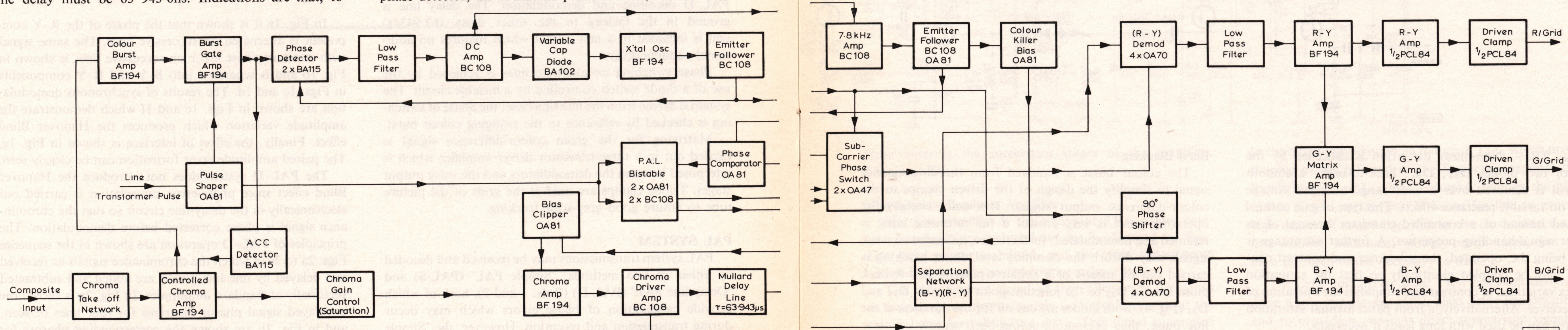
Colour Burst Amp BF194
Burst Gate Amp BF194
Phase Detector 2 x BA115
Low Pass Filter
DC Amp BC 108
Variable Cap Diode BA 102
X'tal Osc BF 194
Emitter Follower BC 108
Line
Transformer Pulse
Pulse Shaper OA81
P.A.L. Bistable 2 x OA81 2 x BC108
Phase Comparator OA 81
Bias Clipper OA81
ACC Detector BA115
Composite Input
Chroma Take off Network
Controlled Chroma Amp BF 194
Chroma Gain Control (Saturation)
Chroma Amp BF 194
Chroma Driver Amp BC 108
Mullard Delay Line τ=63·943μs
7·8 kHz Amp BC108
Emitter Follower BC 108 OA 81
Colour Killer Bias OA81
(R - Y) Demod 4 x OA70
Low Pass Filter
R - Y Amp BF194
R - Y Amp 1/2PCL84
Driven Clamp 1/2PCL84
R/Grid
Sub-Carrier Phase Switch 2 x OA47
90° Phase Shifter
G - Y Matrix Amp BF 194
G - Y Amp 1/2PCL84
Driven Clamp 1/2PCL84
G/Grid
Separation Network (B-Y)(R - Y)
(B - Y) Demod 4 x OA70
Low Pass Filter
B - Y Amp BF 194
B - Y Amp 1/2PCL84
Driven Clamp 1/2PCL84
B/Grid
a 4772A

Fig. 3—Block diagram of decoder

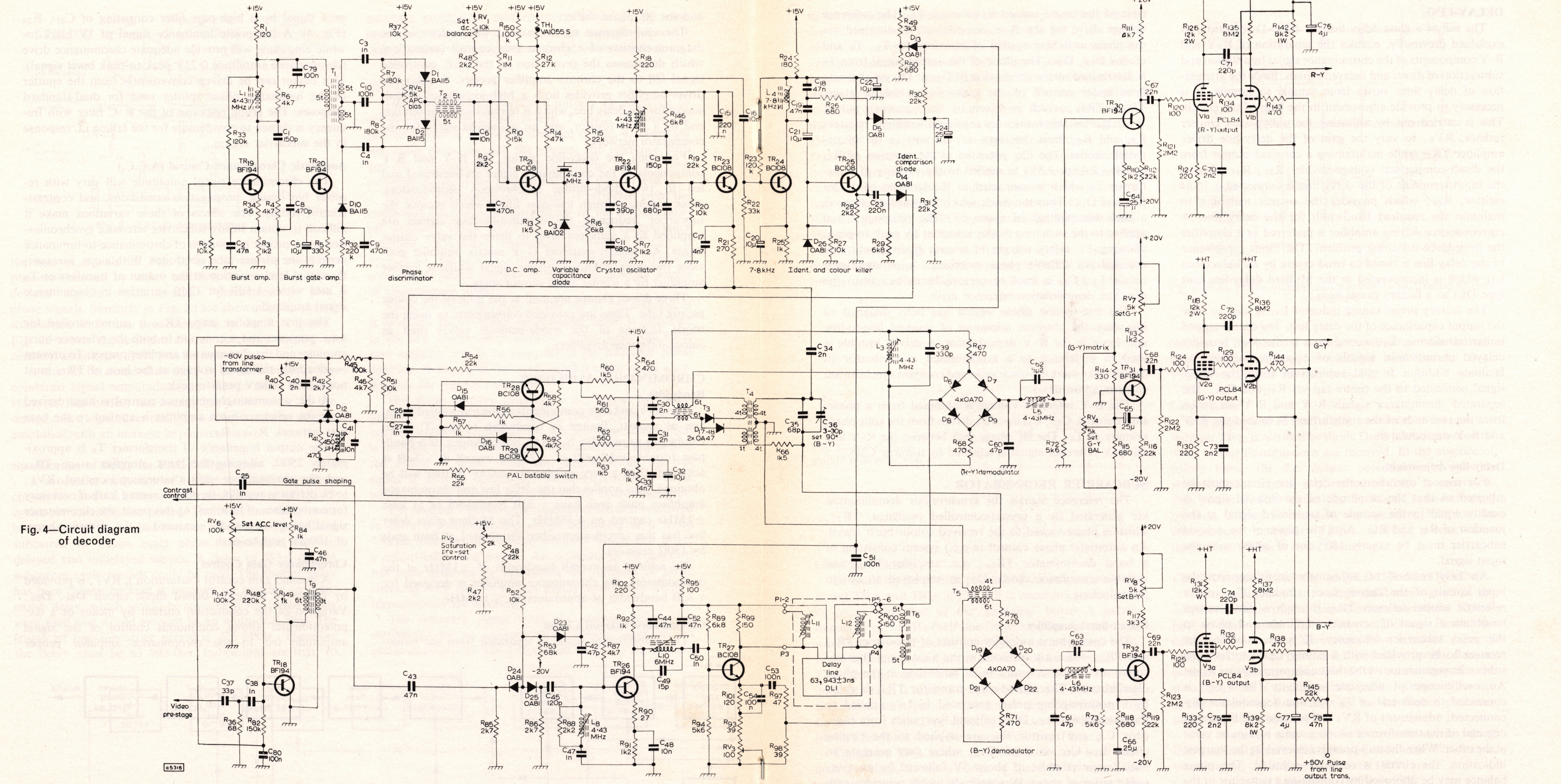
Burst amp.
Burst gate-amp.
Phase discriminator
APC bias
Set d.c. balance
D.C. amp.
Variable capacitance diode
Crystal oscillator
7·8kHz
Ident. comparison diode
Ident. and colour killer
(R−Y) output
(G−Y) output
(B−Y) output
(G−Y)matrix
Set G−Y BAL.
(R−Y)demodulator
(B−Y) demodulator
Set 90° (B−Y)
R−Y
G−Y
B−Y
PAL bistable switch
−80V pulse from line transformer
Gate pulse shaping
Contrast control
Set ACC level
Saturation pre-set control
Video pre-stage
Delay line 63,943±3ns DL1
+50V Pulse from line output trans.
PCL84
a5316

Fig. 4—Circuit diagram of decoder

TR$_{26}$, TR$_{27}$. Non-linear distortion is cancelled by the use of two diodes D$_{24}$, D$_{25}$, back-to-back; a smooth control is achieved over a wide range of input voltage with no variable reactance effects. This type of gain control is used instead of a controlled transistor because of its better signal-handling properties. A further advantage is that being d.c. operated, the subcarrier and contrast controls may be coupled electrically so that the saturation tracks variations in contrast and simplifies the operation of the receiver. Alternatively, a front panel manual saturation control can be used with long leads if necessary.

Burst Blanking

The colour burst is removed from the chrominance signal to simplify the design of the driven clamps in the colour-difference output stages. The exact clamp-pulse operating point is very critical if the reference burst is retained and demodulated; furthermore, h.f. noise on weak signals may disturb the clamping level. Burst blanking is carried out by means of a negative-polarity line flyback pulse fed via D$_{23}$ to the junction point of diodes D$_{24}$ and D$_{25}$ (Fig. 4). Both diodes are cut off for the duration of the line pulse, thus preventing colour-burst signals or noise from entering the succeeding stages of the amplifier, TR$_{26}$ and TR$_{27}$.

Chrominance Bandpass Amplifier

The first amplifier is the transistor TR$_{26}$ whose base-circuit capacitance is tuned-out by L$_8$ damped by R$_{88}$. The stage gain is stabilised, and the input capacitances reduced, by an unbypassed emitter resistor R$_{90}$.

The chrominance signal at the collector of TR$_{26}$ has an amplitude of approximately 0·5V peak-to-peak at the colour burst for full output drive. This signal is coupled to the next stage through an inductor, L$_{10}$, which provides shaping at the h.f. end of the frequency-response curve. Parallel-tuning of L$_{10}$ by C$_{49}$ further reduces the gain at 6MHz (sound subcarrier). It is not feasible to provide a high degree of sound rejection in the chrominance amplifier without additional sharply-tuned traps, but these have not been found necessary to date.

The delay-line driver stage TR$_{27}$ has been designed to drive a low-impedance, 150Ω, glass delay-line circuit DL1 and to provide a constant direct-comparison signal.

DELAY-LINE

The use of a glass delay line for PAL–D reception, as explained previously, enables the separation of R–Y and B–Y components of the chrominance signal by addition and subtraction of direct and delayed signals. Since the attenuation of delay lines varies from sample to sample, it is necessary to provide adjustment in the gain of the circuit. This is carried out by adjusting the unbypassed emitter resistor, RV_3, to vary the gain of the delay-line driver amplifier TR_{27} while maintaining a constant output from the direct-comparison voltage divider R_{97}, R_{98}. Across the input terminals of the delay line is connected a 150Ω resistor, R_{99}, which provides the correct matching to maintain the required bandwidth for the delay line. A current-source driving amplifier is preferred as it simplifies the impedance-matching problem. The input capacitance of the delay line is tuned to band centre by an inductance L_{11} which is incorporated in the Mullard delay-line unit type DL1 as a factory preset item.

The factory preset tuning inductor L_{12} is used to tune the output capacitance of the delay line. The centre-tapped bifilar transformer T_6, wound on a ferrite core, provides delayed chrominance signals of opposite polarities to facilitate addition and subtraction from the direct signal connected to the centre tap via R_{97} and R_{98}. The separated chrominance signals R–Y and B–Y are taken from the two ends of the transformer T_6 to feed the R–Y and B–Y demodulators.

Delay-line Adjustment

For correct operation, the delay-line circuit must be adjusted so that the amplitude of the delayed signal is exactly equal to the sample of undelayed signal at the junction of R_{97} and R_{98}. Also, the phase of the delayed subcarrier must be exactly 180° out of phase with the input signal.

An easy method of adjustment is to connect the input circuit of the chrominance amplifier C_{43} to the reference emitter-follower TR_{23} through a 10kΩ resistor to obtain a signal of constant amplitude and phase at the exact subcarrier frequency. It is essential for the receiver to be provided with a colour signal to lock the subcarrier regenerator whilst this adjustment is being made. An oscilloscope of adequate sensitivity (10mV/cm) is connected to each end of T_6 with the demodulator disconnected; adjustment of RV_3 will provide a null-point at one end of the transformer winding and a maximum value at the other. When the null-point is achieved, at the sharpest indication, the circuit is correctly adjusted. The phase balance may be improved by connecting a capacitor of the order of 100pF across R_{97} or R_{98}; this allows for circuit delay errors outside the delay line. The factory preset inductors L_{11} and L_{12} are adjusted for best performance with respect to all the delay-line parameters and should not be adjusted for delay equalisation.

SYNCHRONOUS DEMODULATION

Diode-bridge demodulators are used to demodulate the R–Y and B–Y phase output signals from the delay-line addition and subtraction networks. These consist of diodes D_{6-9} and D_{19-22} respectively, connected to the opposite ends of the centre-tapped transformer T_6. The reference voltage drive for the R–Y demodulator is obtained via the phase switching system of transformers T_3, T_4 and diodes D_{17}, D_{18}. The phase of the output signal from T_3 is determined by the conduction of D_{17} or D_{18} on alternate lines under control of the scale-of-two bistable stage, TR_{28}, TR_{29}, which is driven by line-frequency pulses. When the bistable transistors conduct alternately, resistors R_{61} and R_{62} limit the 'turn-on' currents in the phase-switch diodes. The d.c. potential at the junction of R_{64} and R_{65} (about 7·5V) is applied to the winding of transformer T_3 which is connected to the junction of diodes D_{17} and D_{18}. Thus the diode which is turned off receives a back bias voltage of about 6V. The reference signal applied to the switching diodes is kept at 6V peak-to-peak, allowing 3V safety margin in reverse biasing, which is essential for reliable phase switching. A parallel-tuned circuit L_3, C_{39} is used to remove harmonics from the switched demodulation-reference drive.

The line-by-line phase switch has been designed to introduce the absolute minimum of residual line-to-line unbalance in the R–Y demodulator. A driven bistable is used in preference to a synchronised multivibrator to obtain unity mark-to-space ratio and constant synchronism without adjustments.

The B–Y reference voltage is obtained from a phase-shift network C_{35}, C_{36} and R_{66} driven from the split-phase primary of T_4. The 90° phase shift between the R–Y and the B–Y reference signal is adjusted by trimmer C_{36}.

SUBCARRIER REGENERATOR

The reference signals for synchronous demodulation are generated by a crystal-controlled oscillator, TR_{22}, which is phase-locked to the received colour-burst signal. An automatic phase control (a.p.c.) system consisting of a burst discriminator TR_{20}, d.c. amplifier TR_{21} and variable-capacitance diode, D_3, is employed to obtain phase-locking.

Colour-burst Amplifier

The colour-burst amplifier consists of transistors TR_{19} and TR_{20} which are included in the a.c.c. loop, thus ensuring an almost constant burst amplitude at the phase discriminator. The second-stage transistor TR_{20} is gated by a positive-going pulse, generated in L_7, applied to the base resistor R_4. Differentiated line pulses from capacitor C_{40} and resistor R_{40} are applied to the ringing circuit L_7, C_{41} via diode D_{12}, where they generate an initial negative pulse of about 5V followed by an overswing pulse of about 3V amplitude which coincides with the colour burst. It is the over-swing pulse which gates the burst. The secondary winding of the phase-splitting transformer T_1 is connected to the phase-discriminator diodes D_1 and D_2 and also to the a.c.c. rectifier D_{10}. The a.c.c. voltage generated at the anode of D_{10} is used to control the variable-gain chrominance take-off stage TR_{18} via R_{32}, R_{82}, maintaining an approximately constant 10V peak-to-peak burst voltage at the discriminator diodes.

The reference signal from the crystal-controlled oscillator TR_{22} is fed via the emitter-follower buffer stage TR_{23} to the demodulator and also to the burst-phase discriminator via transformer T_2. The error signal is fed to the base of the d.c. amplifier transistor TR_{21} which controls the variable-capacitance diode D_3. The 7·8kHz half-line-frequency signal is also taken from the collector of this transistor to the phase-identity circuit. The d.c. amplifier is biased by the preset phase control RV_1 so that, with the burst amplifier disconnected, a reverse voltage of about 5V is applied to the variable-capacitance diode D_3. The resultant effective value of capacitance must be such that the crystal oscillates at almost exactly subcarrier frequency (that is, without phase-lock); reconnection of the burst should then cause phase-lock. Finally, RV_5 is adjusted to obtain a symmetrical holding operation about the centre of reference phase.

The hold-in range obtained from this system is approximately 1kHz, with a catching range of 500Hz dependent on the values of the filter components R_9, C_7 (Fig. 5).

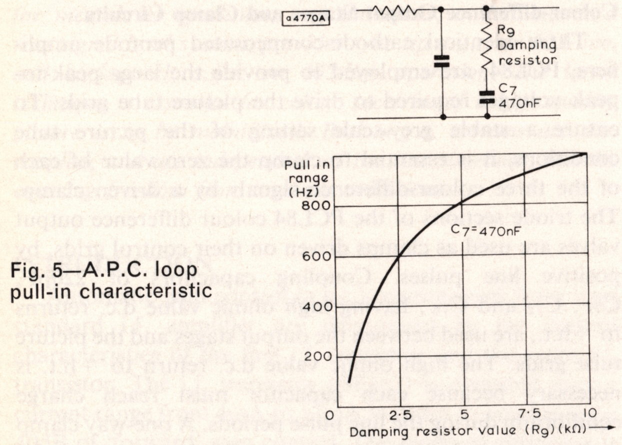

Fig. 5—A.P.C. loop pull-in characteristic

Line Phase-identity

To establish the correct phasing of the reference switch circuit TR_{28} and TR_{29} in Fig. 4 it is necessary to compare its phase with that of the 'swinging' burst. A switch frequency of 7·8kHz (half-line-frequency) for the reference waveform is obtained by amplifying the 'swinging' burst ripple which is present at the collector of the d.c. amplifier TR_{21} in the sub-carrier regenerator circuit. A tuned amplifier TR_{24} is used to reduce the effects of noise during the colour-burst period. The tuned circuit is formed by L_4 and C_{18}, C_{19}. The effective Q-factor is improved by positive feedback from the emitter-follower TR_{25}.

Transistor TR_{25} is not provided with any base bias and, therefore, in the absence of the 7·8kHz signal, its current is zero. When the 7·8kHz signal is generated by the phase detector and applied to TR_{24}, the output is rectified by diode D_{26} and the resulting bias applied to TR_{25}. Hence the transistor conducts and produces a 7·8kHz signal at its emitter which is fed back to the tuned circuit at its input. This is controlled positive feedback, and a large-amplitude 7·8kHz signal is produced at the emitter of TR_{25}.

Switch-phase comparison is carried out by the components D_{14}, C_{23}, R_{29} which modify the operation of the bistable switch steering circuit D_{15}, R_{54}. In correct phase operation, the triggering of the bistable switch is not affected, but if the phase is wrong, the driving pulse through C_{26} is suppressed by the blocking bias through D_{14}. Typical waveforms are shown in Fig. 6.

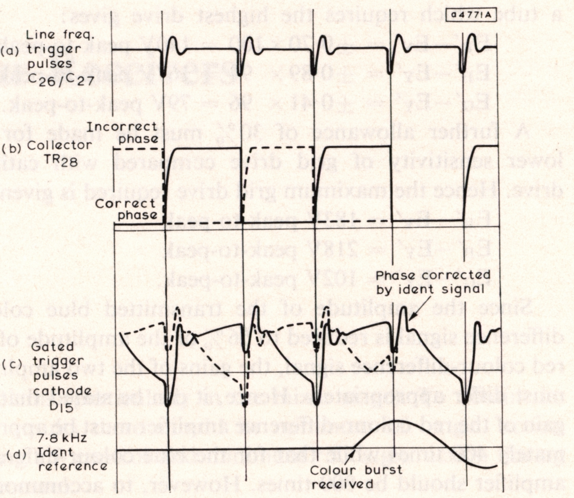

Fig. 6—PAL phase-comparison waveforms illustrating phase-correction

Colour Killer

The peak value of the 7·8kHz waveform at the emitter-follower TR_{25} is rectified by diode D_5 to provide a potential when colour transmissions are received. In the absence of colour burst, the d.c. output potential is zero; with normal colour-signals, a potential of 7·5V is generated. This potential, after smoothing by R_{30}, C_{51} and clipping by D_{13}, is used to maintain the operating bias for the chrominance amplifier TR_{26}. During monochrome transmission TR_{26} is non-conducting.

COLOUR-DIFFERENCE AMPLIFIER MATRIXING

The amplitudes of the colour-difference signals at the output terminals of the demodulators are about 500mV peak-to-peak under full drive conditions. Hence the colour-difference amplifiers must have nominal gains of at least 400 times to provide full grid drive for the electron guns of the picture tube. The drive requirements for the three grids of a contemporary colour-picture tube are calculated in the following way for luminance potentiometer drive at the cathode.

For a correct grey-scale with cathode drive, taking into account picture tube spreads, the range of voltages, when the cut-off voltages are set to 110V, are:

Red cathode	100V to 87V
Green cathode	96V to 76V
Blue cathode	94V to 74V.

In a practical circuit a wider range of adjustment than this should be provided to allow for additional component spreads and tube life.

From the signal specification for fully saturated colour-bar signals:

$E_R'-E_Y' = 0{\cdot}70E_Y'$ (Red colour-difference)
$E_B'-E_Y' = 0{\cdot}89E_Y'$ (Blue colour-difference)
$E_G'-E_Y' = 0{\cdot}41E_Y'$ (Green colour-difference).

Allowance for different cathode drive signals (E_Y) for a tube which requires the highest drive gives:

$$E_R'-E_Y' = \pm 0{\cdot}70\times 100 = 140\text{V peak-to-peak}$$
$$E_B'-E_Y' = \pm 0{\cdot}89\times 94 = 167\text{V peak-to-peak}$$
$$E_G'-E_Y' = \pm 0{\cdot}41\times 96 = 79\text{V peak-to-peak.}$$

A further allowance of 30% must be made for the lower sensitivity of grid drive compared with cathode drive. Hence the maximum grid drive required is given by:

$$E_R'-E_Y' = 183\text{V peak-to-peak}$$
$$E_B'-E_Y' = 218\text{V peak-to-peak}$$
$$E_G'-E_Y' = 102\text{V peak-to-peak.}$$

Since the amplitude of the transmitted blue colour-difference signal is reduced to 56% of the amplitude of the red colour-difference signal, the gains of the two amplifiers must differ appropriately. Hence, it can be stated that the gain of the red colour-difference amplifier must be approximately 400 times while that for the blue colour-difference amplifier should be 800 times. However, to accommodate the spread in tubes it is necessary to provide a range of adjustment of the blue and green drive voltages relative to a fixed red drive voltage by means of variable resistors in the collector circuits of the amplifiers.

Colour-difference Preamplifier and Matrix Circuits

The green colour-difference signal is generated by emitter matrixing in the circuit containing transistors TR$_{30}$, TR$_{31}$ and TR$_{32}$ Fig. 4; amplified red and blue colour-difference signals are obtained at the collectors of TR$_{30}$ and TR$_{32}$ and the green signal at the collector of TR$_{31}$.

Since the output stages are each designed for a stable gain of approximately 40 times, it is necessary to provide peak-to-peak control-grid drive voltages of 4·5, 5·5, 2·6V for red, blue, and green colour-difference signals respectively. In fact, the preamplifiers are capable of fully driving all three output stages as required for an equal-luminance drive system. (This would be the case where the sensitivities of the electron guns of the picture tube are modified by cathode negative feedback or variation of the first anode voltage to provide the correct grey scale ratio when three equal-luminance drive signals are applied.)

The matrix G–Y resistors R$_{114}$, R$_{115}$, and the preset variable RV$_4$ are proportioned so that, with R–Y and B–Y voltages in the ratio in which they appear at the demodulator output terminals, a G–Y signal is generated in the collector circuit of transistor TR$_{31}$. Theoretically:

$$-(E_G'-E_Y') = 0{\cdot}51(E_R'-E_Y')+0{\cdot}186(E_B'-E_Y')$$

so that the theoretical ratio of $(E_R'-E_Y')$ to $(E_B'-E_Y')$ to give $-(E_G'-E_Y')$ is 0·51/0·186. However, since the amplitude of $(E_B'-E_Y')$ as received is 0·56 $(E_R'-E_Y')$, then the ratio of $(E_R'-E_Y')$ to $(E_B'-E_Y')$ required to give $-(E_G'-E_Y')$ is

$$\frac{0{\cdot}51}{0{\cdot}186}\cdot\frac{0{\cdot}56}{1} = \frac{1{\cdot}54}{1}.$$

Hence the ratio of the resistance between the emitters of TR$_{32}$ and TR$_{31}$ should be 1·54 times that between the emitters of TR$_{31}$ and TR$_{30}$. In practice, the position of the slider of the potentiometer RV$_4$ is adjusted on colour-bar signals to give the correct $(E_G'-E_Y')$ waveform when viewed at the collector of TR$_{31}$. Two a.c. coupled emitter resistors R$_{110}$ and R$_{118}$ are used to set the gain of the red and blue colour-difference stages independently from the green matrix setting, and are chosen to give approximately equal-maximum red and blue signals. The d.c. stability of the three pre-stage amplifiers is ensured by the use of high-value emitter feed resistors taken to the −20V line.

Variable resistors with low power ratings are incorporated in the collector load circuits of transistors TR$_{31}$ and TR$_{32}$ to provide adjustment of the blue and green colour-difference signals relative to the red colour-difference signal for different picture tube drive requirements.

Emitter matrixing with three preamplifiers is preferred to cathode matrixing in the valve output stages as it enables the use of high-frequency cathode compensation, high voltage gain and cheaper drive adjustments. Cross-talk occurs in the emitter matrixed circuit but it may be reduced to negligible proportions, if required, by the connection of neutralising resistors (approximately 150kΩ) from the collector of TR$_{30}$ to the emitter of TR$_{32}$, and from the collector of TR$_{32}$ to the emitter of TR$_{30}$.

Colour-difference Output Stages and Clamp Circuits

Three identical cathode-compensated pentode amplifiers, PCL84, are employed to provide the large peak-to-peak voltages required to drive the picture tube grids. To ensure a stable grey-scale setting of the picture tube conditions, it is essential to clamp the zero value of each of the three colour-difference signals by a driven clamp. The triode sections of the PCL84 colour difference output valves are used as clamps driven on their control grids, by positive line pulses. Coupling capacitors of 220pF, C$_{71}$, C$_{72}$ and C$_{74}$, having high ohmic value d.c. returns to +h.t., are used between the output stages and the picture tube grids. The high ohmic value d.c. return to +h.t. is necessary because each capacitor must reach charge equilibrium during the line pulse periods. A one-way clamp such as a triode is limited in its effectiveness for some types of scene since negative variations in d.c. level can only be corrected slowly: the choice of the positive-return resistors R$_{135}$, R$_{136}$, R$_{137}$ is a compromise between line-period slope and clamp recovery time.

TRANSFORMER CONSTRUCTION

All the transformers in the decoder are wound on Mullard FX2249 Ferroxcube cores. These consist of small rectagular blocks with two parallel holes. The windings are threaded through these holes so that the material between the holes forms the core.

The wire used is 38 s.w.g. T.N.A. wire in all cases. The numbers of turns are noted on the circuit diagram 2t, 5t etc. For convenience, 2, 3 or 4 wires of different colours may be threaded simultaneously according to the number of windings or parts of windings.

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A.G.C. for Monochrome and Colour Receivers

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The overall performance required of an a.g.c. system is discussed and consideration is given to circuit techniques for control of the r.f. and first i.f. amplifier stages with suitable r.f. delay, and without requiring the use of close-tolerance components.

Two video signal processing circuits are described. One is for mean-level operation, and the other, a dual-standard true signal level system, provides sync tip a.g.c. on 625-line, and back-porch a.g.c. on 405-line operation. The latter technique is essential for colour receivers if a high quality picture is to be maintained. Both a.g.c. systems are d.c. coupled, and are independent of the line timebase, thereby ensuring freedom from lock-out conditions.

INTRODUCTION

Automatic gain control (a.g.c.) requirements for a dual standard i.f. amplifier are determined by the control characteristics of the first i.f. transistor and the tuner r.f. transistor. The i.f. transistor (BF167) is operated over a current range from 4mA to 13mA in order to achieve some 40dB of 'forward' gain control. The mode of operation is partly current control and partly voltage control and calls for a low impedance a.g.c. circuit. Control range limits are fixed by the correct choice of emitter resistor. The minimum base voltage (at maximum gain) and the extent of bottoming (at minimum gain) are set by a preset potentiometer. These circuit limits give an accurately defined range of i.f. control with different samples of i.f. transistor having spreads in current gain versus emitter current characteristics.

The r.f. transistor (BF180) has similar requirements but the maximum control need not be defined, as the major requirement is to ensure that the signal handling is not impaired by too large an i.f. gain reduction before transfer of control.

TUNER DELAY CIRCUIT

With the introduction of silicon n-p-n transistors in the tuner it is not possible to use the delay techniques derived from a valve positive h.t. line as is used with germanium transistor tuners, since a high-potential negative supply is required.

A new circuit technique must therefore be used. With an ideal a.g.c. circuit, as the aerial signal increases, a.g.c. is first applied to the i.f. stage to give an improved signal-to-noise ratio and is then transferred to the r.f. stage at higher signal levels to safeguard against signal handling problems (particularly in the mixer stage). To obtain the best results there should be minimum i.f. a.g.c. action during r.f. control and minimum r.f. a.g.c. action during i.f. control.

A simple method of ensuring little interaction of a.g.c. between the r.f. and i.f. stages is by coupling them to the control circuit by diodes as shown in Fig. 1. The a.g.c. action of the i.f. stage is controlled by potential V$_2$ being less than V$_1$ and V$_3$ and acting on diode D$_2$. During this period the r.f. stage is isolated by diode D$_1$ being reverse biased. With D$_1$ reverse biased the r.f. stage base potential is set by the potential divider R$_2$, R$_3$ to give maximum gain and optimum noise performance.

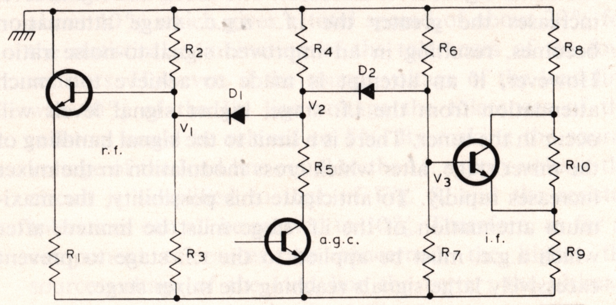

Fig. 1—A.G.C. delay circuit using diodes

The a.g.c. action of the i.f. stage stops when the a.g.c. potential V$_2$ exceeds the quiescent potential V$_3$ of the potential divider R$_6$, R$_7$. These resistors are chosen to operate the i.f. stage at minimum gain. The a.g.c. action of the r.f. stage starts when potential V$_2$ exceeds the quiescent potential V$_1$ of the potential divider R$_2$, R$_3$. These resistors are chosen to operate the r.f. stage at maximum gain. The transfer of a.g.c. action from the i.f. stage to the r.f. stage can therefore take place provided that the quiescent potentials V$_1$ and V$_3$ of the two potential dividers are equal. In practice a slight overlap of a.g.c. action is preferable and will be discussed later in this article in conjunction with tolerances of the components.

This circuit technique requires an additional diode when compared to previous circuits using germanium transistors where the delay was obtained from the valve h.t. line, but has the advantage of having less a.g.c. interaction between the tuner and i.f. stages. Furthermore, this circuit operates entirely from the existing l.t. supply for the tuner and the i.f. stages and does not need a low impedance potential divider to derive the delay potential. The power requirements of the a.g.c. circuit are therefore less and, furthermore, by selecting a suitable load resistance for the a.g.c. amplifier the variation of current taken can be arranged to compensate approximately for the change of currents in the i.f. and tuner stages during a.g.c. operation. This property of giving an almost constant load to the l.t. supply may be important when considering the effects of supply potential variations on the tuner oscillator stability.

CONSIDERATION OF A.G.C. TIME-CONSTANT

In an efficient a.g.c. system the overall loop gain should be high to prevent appreciable changes in detector output with varying aerial signal strengths. The filtering time-constant required in the a.g.c. loop, to prevent fluctuations due to hum and interference voltages, is determined by the maximum slope of the a.g.c. characteristic. For optimum operation it is therefore desirable to match the r.f. and i.f. gain control characteristics at their steepest slopes of loop gain. In a complete design the operation must be checked with limit components over the full control range to ensure that the time-constant is adequate and the system completely stable.

VARIATIONS IN MAXIMUM ATTENUATION OF I.F. STAGE

Initially a.g.c. is applied only to the i.f. stage to maintain a nearly constant output from the video detector as the aerial signal level increases. The more this signal level increases the greater the i.f. a.g.c. stage attenuation becomes, resulting in an improved signal-to-noise ratio. However, if an attempt is made to achieve too much attenuation from the i.f. stage, higher signal levels will occur in the tuner. There is a limit to the signal handling of the mixer stage, after which cross modulation in the mixer increases rapidly. To anticipate this possibility, the maximum attenuation of the i.f. stage must be limited, after which a.g.c. must be applied to the r.f. stage to prevent excessively large signals reaching the mixer stage.

The limit for the maximum permitted attenuation of the i.f. stage must therefore allow for all spreads of stage gain between the mixer input and the video detector output. With typical designs of i.f. amplifiers and tuners the combined spread in gain of the non-controlled stages could be ±6dB. However, the spread in gain of a controlled stage such as the first i.f. stage, when forward biased to give a nominal attenuation of 30dB with nominal resistors, can be larger. This spread in the first i.f. stage is probably about ±8dB if the d.c. conditions of the transistor do not vary by more than ±10% due to the resistor tolerances, with a further spread of about ±6dB due to the transistor tolerances. This overall spread is then the combination of these spreads (±6dB, ±8dB, ±6dB) to which must be added any increase in the detector output level during r.f. a.g.c. action

Statistical addition of these spreads results in ±12dB, but this might not be considered safe, because of the serious consequences of cross modulation. If, however, ±12dB is considered to be a safe estimation then the nominal signal into the mixer stage during r.f. a.g.c. would have to be at least 12dB down on the level which causes unacceptable cross modulation, and the spread in this signal level would be ±12dB.

Such a reduction in input signal level to the mixer stage will reduce the signal-to-noise ratio of the receiver, so that in the worst case a signal-to-noise ratio of less than 40dB can be expected, which is considered unacceptable.

To reduce these spreads in gain a preset control for the maximum attenuation of the i.f. a.g.c. stage is therefore desirable. The most convenient method of presetting the maximum attenuation of the controlled i.f. amplifier is by varying the value of R_7 (Fig. 1). A small change in this resistor has a large effect on the maximum attenuation of the stage but very little effect on the maximum gain setting since R_7 is then shunted by the very much lower resistance of R_5.

The preset resistor can be adjusted to give a suitable sensitivity of the i.f. amplifier when the diode D_2 is reverse biased. An alternative method of adjustment in a complete receiver would be to select a suitable aerial signal at which the r.f. stage should start to attenuate and then adjust R_7 to give the appropriate d.c. potential across the r.f. stage emitter resistor R_1. The only remaining gain spread to be considered now as far as the signal handling of the mixer stage is concerned is the spread of gain of the mixer stage itself; but this is usually small.

DETERMINING OPTIMUM LOAD LINE OF A.G.C. STAGES WITH REGARD TO SIGNAL HANDLING

A.G.C. can be applied to a transistor either by varying the d.c. potential across it (voltage control) or by varying the current flowing through it (current control). In practical a.g.c. circuits a combination of both is used and the degree of current or voltage control depends on the slope of the load line. In practice, for appreciable attenuations, the greater the current flowing in a transistor for a given attenuation, the better the signal handling. This phenomenon is best understood by considering the simple equivalent circuit for the input of the transistors with some resistance $r_{bb'}$ between the base terminal and the effective emitter base diode; the latter being the non-linear element which mainly causes the distortion of the a.c. signal. The impedance of this diode falls as the d.c. flowing through the emitter of the transistor rises. The input of the transistor, therefore, acts as a variable potential divider; and for a given signal handling of the effective emitter base diode the signal handling at the transistor input terminals increases as the d.c. flowing through the emitter increases. Since the best signal handling occurs at the largest permissible emitter current it is therefore preferable to operate a.g.c. stages as close to the maximum permitted dissipation as possible. Typical curves of constant attenuation proportional to current and voltage are shown in Fig. 2.

I.F. Stage

The signal handling property of the i.f. stage is probably most important in the vicinity of the nominal value of the maximum required attenuation, since the i.f. stage operates at this point when the receiver is receiving strong signals (that is, throughout the whole of the r.f. a.g.c. range).

The optimum load line is then one which is tangential to the maximum permitted dissipation at this attenuation. Care should be taken when calculating the maximum permitted dissipation since allowance must be made for tolerances in the resistors and the rail voltage.

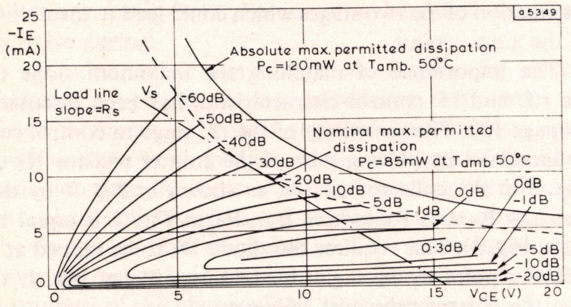

Fig. 2—Typical lines of constant attenuation plotted as I_E versus V_{CE}

R.F. Stage

The signal handling property of the r.f. stage is important over the a.g.c. range of the r.f. stage. For this reason the optimum load line is then one which is tangential to the maximum permitted dissipation near the middle of the available attenuation range, thereby giving the best compromise over the whole range of attenuation.

DETERMINING OPTIMUM LOAD LINE OF A.G.C. STAGES WITH REGARD TO RESISTOR TOLERANCES

From the preceding consideration the source voltage and source resistance of a suitable load line can be determined. Provided that this source voltage is lower than the l.t. supply voltage the appropriate load line can be obtained by using a potential divider across the l.t. supply as indicated by R_1, R_2 in Fig. 3.

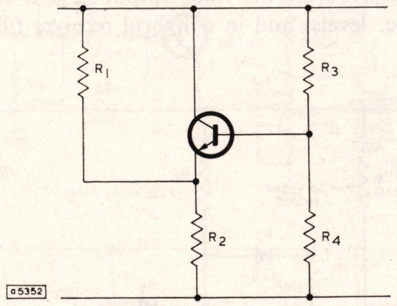

Fig. 3—Controlled stage with source voltage and load line established by potential divider

If, however, the no-load output voltage of this potential divider is very much less than the l.t. supply, then even small tolerances in any of the biasing resistors can result in large variations in the operating current of the transistor especially at small current settings.

R.F. Stage

The setting of the operating point for best noise performance of the r.f. stage is fairly critical. The effects of resistor tolerances can therefore be critical.

The possibility of using additional negative feedback to set this operating point should therefore be considered as the next logical step since this could avoid the need for a preset resistor. However, since the collector of the tuner transistor is usualy returned to earth, feedback can only be applied to the emitter circuit.

A circuit which employs additional negative feedback is shown in Fig. 4. However, this can have the disadvantage of requiring a very large current through the potential divider R_1, R_2 to give sufficient negative feedback by the action of R_5, particularly when a load line with a low source voltage is required. The circuit of Fig. 3 should therefore be re-examined.

In a typical r.f. stage biased for best noise performance, as in the circuit of Fig. 3, the following resistor tolerances were found to be necessary. For a load line with a source voltage of 60% of the l.t. line voltage, a 2% variation in any resistor gave a variation of the operating current of about 10% which gives a total spread of about 20% for the statistical combination of the tolerances of the four resistors. However, if the source voltage of the load line was 80% of the l.t. line voltage the tolerances of the resistors could be relaxed to 5%. By making the source voltage of the load line equal to the l.t. supply voltage the circuit is simplified to that of Fig. 5, and the resistor tolerances can all be relaxed to 10%. Therefore, as far as component tolerances are concerned, the higher the source voltage of the load line the better; the ultimate being achieved in the circuit of Fig. 5.

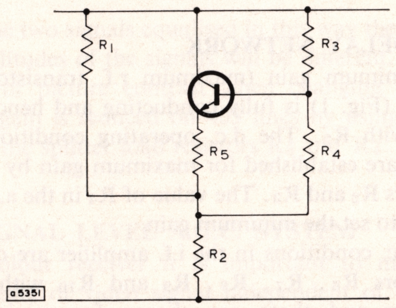

Fig. 4—Controlled stage with additional negative feedback

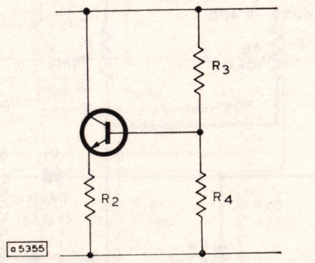

Fig. 5—Controlled stage with l.t. supply potential equal to required source voltage

I.F. Stage

The setting of the operating point for the maximum gain of the i.f. stage is not usually considered to be as critical as the minimum noise point for the r.f. stage. The resultant tolerances will be similar to those given for the r.f. stage. Negative feedback could be obtained from the collector circuit as shown in Fig. 6 but this would correspondingly lower the d.c. input impedance of the stage.

Any errors in the biasing of the maximum attenuation point can be allowed for by the preset resistor (R_7 in Fig. 1) as recommended on page 120.

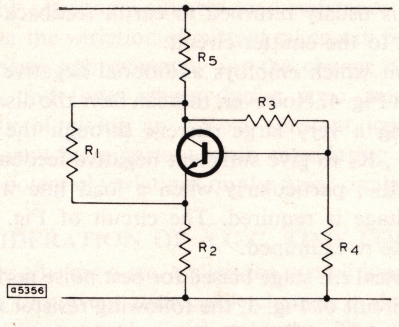
R5
R3
R1
R2
R4
A5356

Fig. 6—Controlled i.f. stage with additional feedback from collector

A.G.C. DELAY NETWORK

At minimum gain (maximum r.f. transistor current) diode D_1 (Fig. 1) is fully conducting and hence R_4 is in parallel with R_2. The d.c. operating conditions for the r.f. stage are established for maximum gain by the choice of resistors R_2 and R_3. The value of R_4 in the a.g.c. circuit is chosen to set the minimum gain.

The d.c. conditions in the i.f. amplifier are determined by resistors R_6, R_7, R_8, R_9 and R_{10} with D_2 non-conducting and these are chosen for minimum gain (maximum transistor current). At maximum gain the a.g.c. transistor is bottomed and D_2 is fully conducting, hence the base of the i.f. transistor is held at a potential determined by R_4 and R_5 in parallel with R_6 and R_7.

The current at which appreciable attenuation starts in the r.f. transistor is approximately double that for the best noise performance. The crossover of a.g.c. from the i.f. to the r.f. amplifier should therefore overlap to such an extent that the r.f. is just starting to attenuate when the i.f. control stops. Allowance should be made for component tolerances to ensure that the overlap does not become too great, thereby causing an excessive combined attenuation of the two stages which could lead to instability of the a.g.c. circuit.

The importance of matching the maximum slope of the r.f. and i.f. control characteristics has been discussed on page 120. The sensitivity of the i.f. stage to control can be increased by placing part of the emitter resistor R_2 of Fig. 3 in the collector circuit, as shown in Fig. 7 by the resistors R_2 and R_5 (where R_2+R_5 in Fig. 7 is equal to R_2 in Fig. 3). This requires the diode D_2 to be tapped at a different point in the a.g.c. load resistor R_4 of Fig. 1, to give the correct crossover of a.g.c.

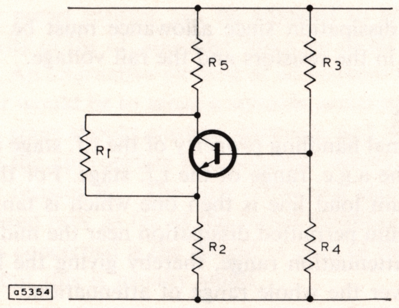
R5
R3
Rf
R2
R4
A5354

Fig. 7—Controlled i.f. stage with increased sensitivity to control

When the desired a.g.c. operation is achieved it is worth considering a slight modification to the a.g.c. load resistors R_4 and R_5 of Fig. 1, so that the current change in the a.g.c. stage will give a substantially constant l.t. load.

DRIVING THE A.G.C. AMPLIFIER

The variation of drive current to the a.g.c. amplifier is generally too large to permit it to be driven from the video detector. Drive from the video output stage is complicated by the d.c. levels, and in a hybrid receiver further complications result from the use of a valve and the effects of valve ageing.

An alternative approach is to employ an emitter follower to provide a low impedance drive from the detector circuit. In a dual standard receiver the system switching can be simplified and the problems of harmonic radiation from the detector reduced by using the transistor as a phase splitter. The a.g.c. amplifier can be driven from the emitter on both standards, and the video signal taken from the emitter or collector as appropriate. A further advantage of the phase splitter when driving a 'high level' contrast control in a receiver with a mean level a.g.c. system is that it reduces the overdrive of the video stage and picture tube on low key scenes, thus minimising 'caption effect' (that is, grid current during peak white causing a shift in the background level).

MEAN-LEVEL A.G.C. SYSTEM

An a.g.c. system, suitable for monochrome receivers, operating on the mean level of the video signal is shown in Fig. 8. The mean level of the video signal developed across R_5, C_1 in the emitter network of the video splitter stage TR_1 is applied directly to the a.g.c. amplifier transistor TR_2. The bias applied to the phase splitter by RV_2 provides the a.g.c. level setting adjustment. If a low-level contrast control (that is, via the a.g.c. system) is used, RV_2 becomes the contrast control. Alternatively, a high-level control can be included in the video output stage as a video gain control, RV_8.

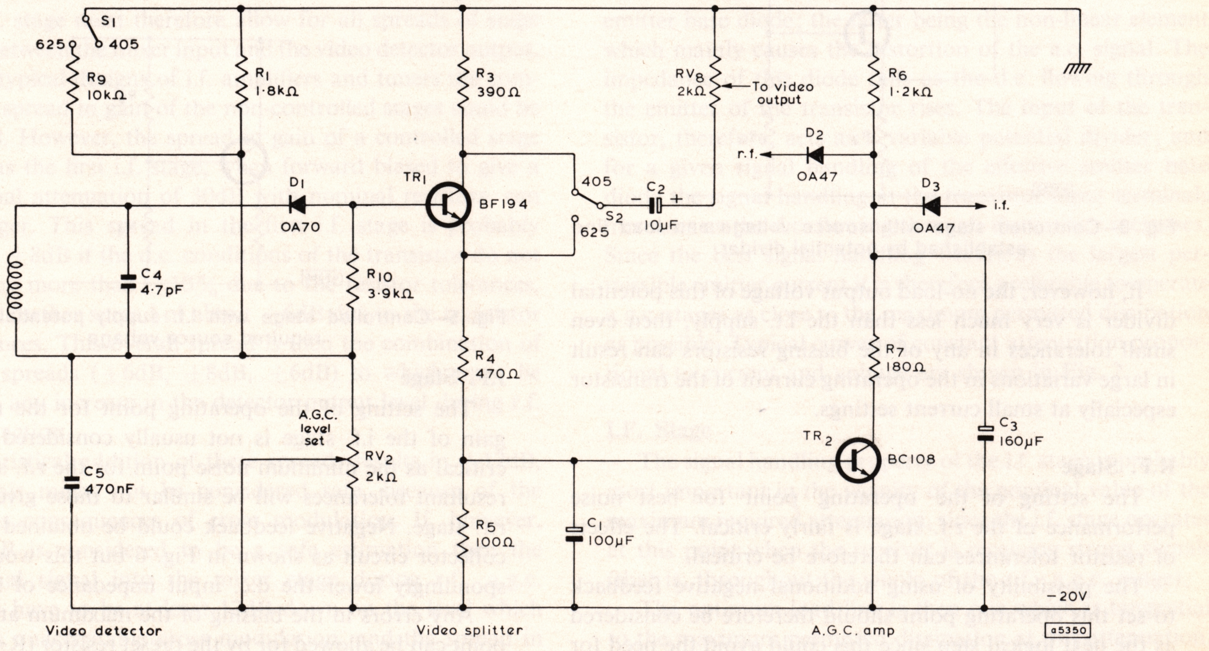
S1
625
405
R9 10kΩ
R1 1·8kΩ
R3 390Ω
RV8 2kΩ
To video output
R6 1·2kΩ
D1 OA70
TR1 BF194
405
S2
625
C2 10µF
D2 OA47
r.f.
D3 OA47
i.f.
C4 4·7pF
R10 3·9kΩ
R4 470Ω
R7 180Ω
A.G.C. level set
RV2 2kΩ
TR2 BC108
C3 160µF
C5 470nF
R5 100Ω
C1 100µF
−20V
Video detector
Video splitter
A.G.C. amp
A5350

Fig. 8—Dual standard mean level a.g.c. circuit

Owing to the differences between the modulation parameters of the 405-line and 625-line signals, an a.g.c. system which established the same mean signal levels at the video detector on both systems would, for average picture scenes, establish a considerably larger peak output on 405 lines. To obtain an adequate detector output amplitude on 625 lines whilst avoiding serious overloading of the last i.f. stage on 405 lines it is necessary to equalise the detector output signals. This is done by increasing the d.c. bias in the splitter transistor on 625 lines by S_1 and R_9. In a complete receiver design this switch operation (S_1) can be combined with an existing 405/625 switching operation.

With the two signals equalised in this way the black-to-white amplitudes of the signals will be different. To avoid a change of picture contrast when changing standards the video gain is reduced on 405 lines by using different values for the splitter load resistors R_3 and R_4.

TRUE SIGNAL LEVEL A.G.C. SYSTEM

In a colour receiver it is important to maintain a constant level of video signal independent of the video information. Since negative modulation is used on the 625-line system the synchronising pulse tips can be used for a.g.c. purposes. To avoid blocking difficulties it is essential to employ a d.c. coupled system which operates on a peak detection principle and which is also independent of the line timebase synchronisation.

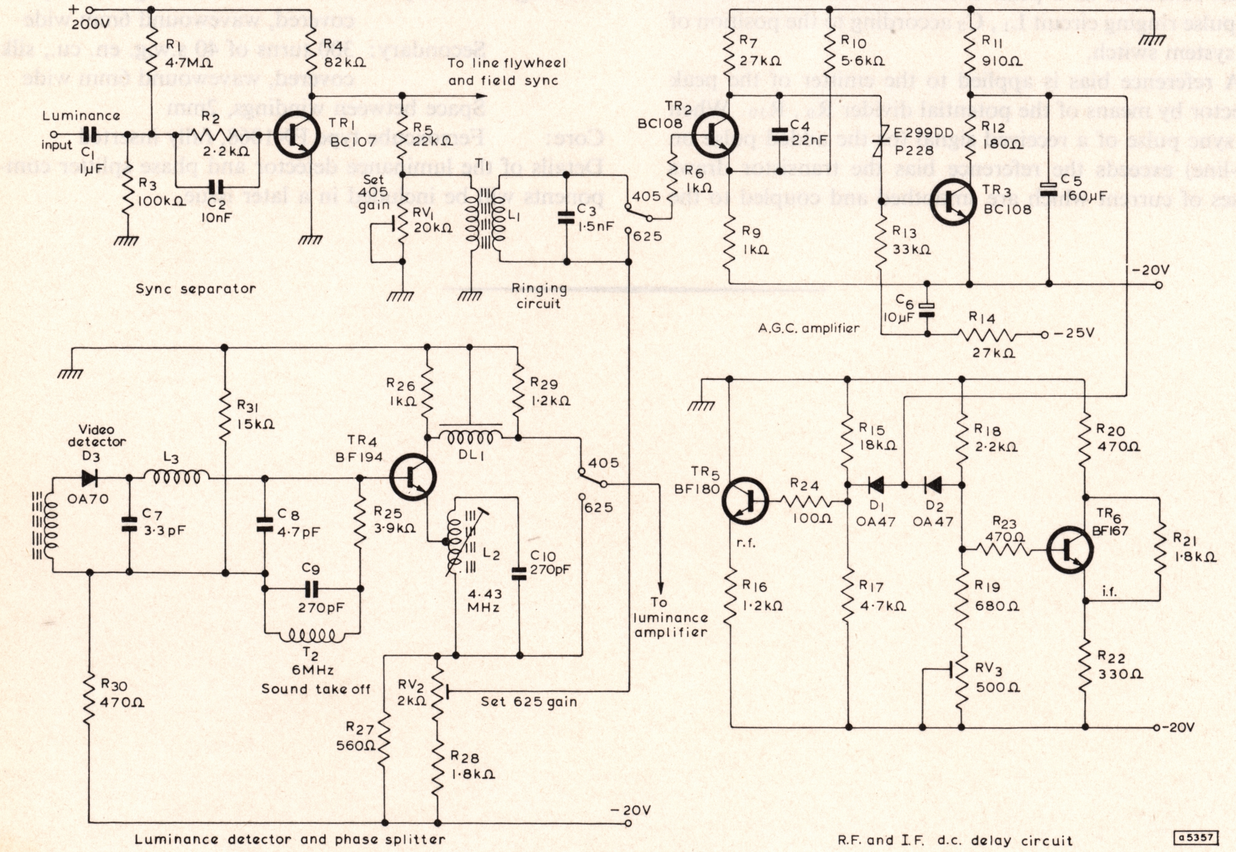
+200V
R1 4·7MΩ
R4 82kΩ
To line flywheel and field sync
Luminance input
C1 1µF
R2 2·2kΩ
TR1 BC107
R5 22kΩ
R3 100kΩ
C2 10nF
Set 405 gain
RV1 20kΩ
T1
L1
C3 1·5nF
Sync separator
Ringing circuit
405
625
TR2 BC108
R6 1kΩ
R7 27kΩ
R10 5·6kΩ
R11 910Ω
C4 22nF
E299DD P228
R12 180Ω
C5 160µF
TR3 BC108
R9 1kΩ
R13 33kΩ
−20V
C6 10µF
R14 27kΩ
−25V
A.G.C. amplifier
Video detector D3 OA70
L3
R31 15kΩ
TR4 BF194
R26 1kΩ
DL1
R29 1·2kΩ
405
625
C7 3·3pF
C8 4·7pF
R25 3·9kΩ
L2
C10 270pF
4·43 MHz
C9 270pF
T2 6MHz Sound take off
To luminance amplifier
R30 470Ω
RV2 2kΩ
Set 625 gain
R27 560Ω
R28 1·8kΩ
−20V
Luminance detector and phase splitter
TR5 BF180
r.f.
R24 100Ω
D1 OA47
D2 OA47
R15 18kΩ
R18 2·2kΩ
R20 470Ω
R23 470Ω
TR6 BF167
R21 1·8kΩ
i.f.
R16 1·2kΩ
R17 4·7kΩ
R19 680Ω
RV3 500Ω
R22 330Ω
−20V
R.F. and I.F. d.c. delay circuit
A5357

Fig. 9—Complete circuit of a true signal level a.g.c. system for colour receiver

To achieve a similar operation on the 405-line positive modulation system the back-porch must be sampled for the black-level reference. This is achieved in the circuit to be described by adding a constant amplitude pulse to the detected (d.c. coupled) video signal, timed to coincide with the back-porch period. Such a pulse is obtained by means of a damped ringing circuit which is excited by the line pulse at the sync separator collector. Owing to the limiting action of the sync separator a nearly constant amplitude pulse is achieved over a wide range of signal strengths; any marginal variations are proportional to signal strength in the correct sense to reinforce the a.g.c. action. The ringing circuit is tuned to a period of approximately 16μs so that the first positive overswing occurs during the back-porch period on a 405-line signal.

An advantage of this sytem is that the system switching in the a.g.c. circuit only requires a changeover switch which selects the direct video signal (625) or the video signal plus sampling pulse (405). When the receiver is being 'tuned in' and the separator may not be operating correctly the system reverts to a mean-level one and hence avoids gating difficulties.

Circuit Description

The complete circuit of a true signal level a.g.c. system used in a colour receiver is shown in Fig. 9. Its operation is as follows:

A proportion of the video signal at the emitter of the phase splitter TR$_4$ is taken from the slider of the preset potentiometer RV$_2$ to the base of the a.g.c. transistor TR$_2$ which functions as a peak detector either directly or via the pulse ringing circuit L$_1$, C$_3$ according to the position of the system switch.

A reference bias is applied to the emitter of the peak detector by means of the potential divider R$_9$, R$_{10}$. When the sync pulse of a received signal (or the added pulse on 405-line) exceeds the reference bias the transistor draws pulses of current which are smoothed and coupled to the output stage TR$_3$. The inclusion of the pulse smoothing capacitor C$_4$ allows the transistor to draw high peak currents without bottoming. The main a.g.c. time-constant is determined by C$_5$ at the output. The level at which a.g.c. action starts is set by adjustment of RV$_2$ which controls the proportion of video signal applied to the a.g.c. circuit. The 405-line signal level adjustment is provided by RV$_1$ across the ringing circuit.

The a.g.c. transistor TR$_3$ is d.c. coupled to the peak detector by means of a v.d.r. and resistor chain. The collector circuit of this transistor is coupled to the tuner and i.f. circuits by two delay diodes (D$_1$ and D$_2$) which determine the range of control for each section.

At low signal inputs TR$_3$ is conducting heavily, thus maintaining D$_2$ in conduction which in turn causes the base potential of the first i.f. transistor TR$_6$ to be held at a low value (that is, high gain condition).

As the signal increases, the driver transistor TR$_3$ conducts less, as does D$_2$, which allows the base potential of the i.f. transistor to rise, thus reducing the i.f. gain. This action continues until D$_2$ is completely cut off by the potential difference between the collector of TR$_3$ and the preset (minimum gain) potentiometer (RV$_3$ and R$_{19}$) in the base circuit of TR$_6$. With the further reduction in current in TR$_3$, due to increase in signal strength, D$_1$ starts to conduct, raising the base potential of the tuner r.f. transistor and thus reducing the overall tuner gain.

Transformer Specification (T$_1$, Fig. 9)

Former: $\frac{1}{4}$in dia. S.R.B.P. tube
Windings: Primary: 600 turns of 40 s.w.g. en. cu., silk covered, wavewound 6mm wide
Secondary: 300 turns of 40 s.w.g. en. cu., silk covered, wavewound 6mm wide
Space between windings, 2mm
Core: Ferroxcube type FX1068, fully inserted

Details of the luminance detector and phase splitter components will be included in a later issue.